Hemraj Meena
Electrical Engineering **Dual Degree (B.Tech. + M.Tech.)**
Indian Institute of Technology Bombay
Specialization: Integrated Circuit and Systems

Examination	University	Institute	Year	CPI / % Credits
Graduation	IIT Bombay	IIT Bombay	2027	6.71 **Core:** 201 | **Total:** 285
Intermediate	TSBIE	NARAYANA JUNIOR COLLEGE	2021	98.20%
Matriculation	BSEAP	NARAYANA EM HIGH SCHOOL	2019	10

Scholastic Achievements

- Recipient of the **Andhra Pradesh Pratibha Award** for extraordinary performance in all the subjects of **BSEAP** ('19)
- Secured a perfect **10/10 GPA** in Class 10 State Board examination conducted by **BSEAP with distinction** ('19)
- Ranked in the **top 2%** among **400k+** students with **98.2%** marks in 12th in **TSBIE** across the state ('21)

Research Experience

Low-Profile L-Band Circularly Polarized Antenna for SATCOM Applications *(Ongoing)*

Guide: Prof. Jayanta Mukherjee | Dual Degree Project (DDP)

- Designed and impedance-matched a **low-profile L-band** cross-dipole bow-tie antenna on Rogers RO4003C, establishing the baseline radiation performance for subsequent reflector integration
- Developed a **linearly polarized configuration** and synthesized an **Artificial Magnetic Conductor (AMC)** surface, achieving **100% L-band coverage** and comparing gain, bandwidth, and profile reduction against a PEC reflector
- Demonstrated that the **AMC** achieves radiation performance better than **PEC** at substantially reduced antenna–reflector spacing, enabling a **low-profile configuration** through engineered in-phase reflection characteristics
- Extended the design to **circular polarization** for orientation-independent operation, achieving **axial ratio below 3 dB** and improving the **axial-ratio** fractional bandwidth from **21.85% to 34.97%** with AMC integration

Cross-Dipole Antenna with AMC for L-Band Applications *(Spring'26)*

Guide: Prof. Jayanta Mukherjee | Research & Development Project (EE 691)

- Successfully simulated a **low-profile** cross-dipole antenna for L-band applications and investigated **Artificial Magnetic Conductor (AMC)** integration for gain enhancement and profile reduction through reflector optimization
- Designed an **L-band AMC unit cell** on **FR4**, with a **1.147–1.899 GHz** reflection-phase range and a **5×5 array**
- Performed full-wave electromagnetic analysis across standalone, **PEC-grounded**, and AMC-integrated configurations, evaluating S_{11}, impedance bandwidth, gain, radiation patterns, and antenna profile for assessment
- Integrated the cross-dipole with the AMC array, achieving **8.69 dBi gain** from 2.63 dBi (**230.42% increase**), **59.9% L-band coverage**, **100% GNSS coverage**, and **25.5% height reduction** to 39.124 mm (AMC) from 52.524 mm (PEC)

Key Projects

Handheld Metal Detector and Rebar Locator *(Spring'25)*

Guide: Prof. Siddharth Tallur | Course: Electronic Design Lab (EE 344)

- Designed a **low-power** analog metal detector using **eddy-current sensing** for buried metal object detection
- Developed a **3 kHz** analog signal chain comprising a Wien bridge oscillator, MOSFET current driver, transmit/receive coils, **INA128** instrumentation amplifier, bandpass filter, and Zener-diode threshold detector
- Built and debugged the hardware prototype, demonstrating reliable metal detection up to 5 cm using a buzzer
- Optimized the design for **low power and low cost** without a microcontroller or display, while addressing practical hardware issues including breadboard limitations, component failure, noise, and coil-size constraints

Dual-Band Wilkinson Power Divider | Course Project *(Autumn'25)*

Guide: Prof. Jayanta Mukherjee | Course: Microwave Integrated Circuits (EE 611)

- Designed a dual-band Wilkinson power divider for **2.4 and 4 GHz** using microstrip transmission lines on **FR-4** ($\epsilon_r = 4.4$, $h = 1.6$ mm) for targeted dual-band operation with **15%** fractional bandwidth across both bands
- Derived circuit parameters using even- and odd-mode analysis, obtaining $Z_1 = 81.57\,\Omega$, $Z_2 = 61.3\,\Omega$, $R = 100\,\Omega$, $L = 2.7$ **nH,** $C = 0.965$ **pF**, and verified the design through TLIN, MLIN, and EM simulations in **Keysight ADS**
- Generated the **microstrip PCB layout** with bends and port assignments, followed by layout-based EM verification and S-parameter analysis across both operating bands for the complete design and performance validation

RISC Processor Design | Course Project *(Spring'24)*

Guide: Prof. Virendra Singh | Course: Microprocessor (EE 309)

- Designed a multicycle datapath using **VHDL** for the instruction set of a **16-bit** computer named IITB-RISC
- Modeled an FSM controller using behavioral modeling and performed **RTL simulations** on datapath and FSM
- Enhanced the design for **17 instructions**, including conditional, immediate, and branch operations

Two-Stage OTA Design with Frequency Compensation | Course Project *(Autumn'25)*
Guide: Prof. Rajesh Zele | Course: CMOS Analog VLSI Design (EE 618)

- Designed a differential two-stage OTA in **Cadence Virtuoso** achieving **54 dB gain**, **126 MHz unity-gain frequency**, 114 V/µs slew rate, and 64–68° phase margin with RC and tracking compensation under an 188 mW power budget
- Verified design performance across **TT/FF/SS process corners** using Spectre, meeting a noise specification of 17 nV/$\sqrt{\text{Hz}}$ at 10 MHz and 600.8 mV_{pp} output swing through detailed DC, AC, transient, and noise analysis
- Developed a full-custom layout (8.425×20.4 µm²) with common-centroid matching and structured routing for critical devices, completing **DRC/LVS** checks and performing Quantus PEX extraction to validate the final layout

4×4 Matrix Fused Multiply-Add (FMA) Accelerator | Course Project *(Autumn'25)*
Guide: Prof. Laxmeesha Somappa | Course: VLSI Design (EE 671)

- Designed a **4-stage** pipelined FMA architecture for 4×4 matrix operations $(A \times B) + C$, comprising input registration, parallel matrix multiplication, accumulation, and saturation stages for efficient computation
- Developed RTL architecture with **16-bit** signed/unsigned arithmetic, matrix parameters, and saturation-based overflow handling, achieving 4-cycle latency and 1 operation/cycle throughput for matrix computations
- Implemented the complete RTL-to-physical-design flow through synthesis, layout, and sign-off checks, achieving **100 MHz** with **2.496 ns setup** and **0.008 ns hold slack**, **177,296.76 μm^2 area**, and **28.78 mW** after routing

Packet-Level Round-Robin Switch Architecture | Course Project *(Spring'26)*
Guide: Prof. Madhav Desai | Course: Algorithmic Design of Digital Systems (EE 789)

- Designed packet-level **arbiter mux/demux FSMs** with counters, guaranteeing packet transfer before switching
- Implemented packet-level round-robin arbitration with priority updates after each packet, eliminating starvation
- Developed three **2×2 switch architectures** using queues, arbiter muxes and demuxes for different routing paths
- Verified all switch designs using **AHIR** testbench and GHDL simulation, confirming correct packet transfers

ECG Amplifier Circuit | Course Project *(Spring'24)*
Guide: Prof. Anil Kottantharayil | Course: Analog Circuits Laboratory (EE 230)

- Developed a comprehensive **ECG (Electrocardiogram)** Amplifier Circuit entirely from scratch, integrating advanced methodologies such as **Right Leg Drive (RLD)** and notch filtering techniques for enhanced performance
- Meticulously engineered the circuit for precise cardiac signal capture, robustness, and **noise** interference mitigation
- Collaborated effectively with peers to collectively troubleshoot challenges and optimized the circuit performance

Technical Skills

Programming	C/C++, Verilog/VHDL, HTML, R, LaTeX
VLSI & EDA Tools	**Ansys HFSS**, **Cadence Virtuoso**, **Keysight ADS**, Quartus Prime, Magic, KiCad, LTspice
Other Softwares	Git, Fusion 360, Blender, Photoshop, DaVinci Resolve

Relevant Courses

Electrical Courses	Electronic Devices, Signal Processing, Electromagnetic Waves, Control Systems, **Radiating Systems***, Microprocessors, Communication Systems, **VLSI Design**, **CMOS Analog VLSI Design**, Digital Signal Processing, **Testing and Verification of VLSI Circuits**, **Algorithmic Design of Digital Systems**, **Microwave Integrated Circuits**, **Advanced Antennas**, Topics in Cryptology, Introduction to MEMS
Mathematics & CS	Calculus I & II, Linear Algebra, Differential Equations, Complex Analysis, Introduction to Data Science and Machine Learning, Wavelets, Fundamentals of Digital Image Processing, Probability and Random Processes
Laboratories	Analog Lab, Digital Circuits Lab, Microprocessors Lab, Electronic Design Lab
Interdisciplinary	Economics, Makerspace, Joint Biomechanics, Planetary Sciences, Terrestrial Ecology

** Ongoing; expected to be completed by Nov'26.*

Position Of Responsibility

Teaching Assistant | **EE 611 – Microwave Integrated Circuits** *(Ongoing)*
Department of Electrical Engineering, IIT Bombay | Prof. Jayanta Mukherjee

- Assisting with **projects, student queries, and course logistics** and thereby ensuring smooth conduct of the course

Extra-Curriculars

- **Sports & Leadership:** Captained football to **Gold at Zonals** and **Bronze at District level**; captained kabaddi at zonal inter-school tournaments with 20+ schools and won **Silver at IIT Bombay GC'24** for H-5; completed year-long cadet training with 2 MAH ENGR REGT **NCC**, IIT Bombay.
- **Social Outreach:** Participated in Pulse Polio Abhiyaan campaigns across rural Rajasthan; contributed **40 kg of old books** through Swachh Andhra Abhiyaan and collected **150+ kg of plastic waste** in NCC lake-cleaning drives.
- **Cultural Engagement & Interests:** Selected twice for inter-school speech competitions; secured 1st place in school essay writing and participated in district-level skits and speeches, with interests in photography and videography.
- **Distinctions:** Served as House Captain and placed in the **top 10% in AMTI** for three consecutive years; awarded **Student of the Year 2017–18** by LIC and selected among the **top 5%** for the KNOW FOR SURE quiz by Britannica, Hyderabad.